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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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09/822,665

03/30/2001

Jeffrey J. Holm

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02/25/2004

LSI LOGIC CORPORATION  
1621 BARBER LANE  
MS: D-106 LEGAL  
MILPITAS, CA 95035

EXAMINER

THAI, XUAN MARIAN

ART UNIT

PAPER NUMBER

2111

DATE MAILED: 02/25/2004

4

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/822,665

Applicant(s)

HOLM ET AL

Examiner

XUAN M. THAI

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-- The MAILING DATE of this communication appears on the cover sheet with the corresponding address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 30 March 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 March 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 2.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

### **DETAILED ACTION**

1. This is in response to a nonprovisional application for patent filed on March 30, 2001.

Claims 1-20 are presented for examination.

### ***Drawings***

2. This application, filed on 3/30/2001, lacks formal drawings. The informal drawings filed in this application are acceptable for examination purposes. Applicant is required to submit new formal drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

### ***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-7, 11-16, and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Thaller et al. (USPN 5555382; Thaller).

As per claims 1, 11 and 20, Thaller discloses a system [10] and method comprising: a bus [28]; at least one master [e.g. 14,16]; and a first circuit [256; fig. 3B] configured to (i) grant a bus mastership [col. 54, lines 48-56], (ii) present a first transfer signal to said bus [col. 54, lines 48-

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56; col. 57, lines 5-7], (iii) remove said mastership from all masters [e.g. col. 56, lines 30-35] and (iv) present an idle transfer signal [col. 56, lines 30-42].

As per claims 2 and 12, Thaller discloses wherein (i) the first circuit is configured to detect [col. 63, lines 12-14 and 18-19] when zero masters of said at least one master are able to use the bus; (ii) removing mastership from all masters [col. 63, lines 18-21].

As per claims 3-6 and 13-16, Thaller discloses wherein the masters are involved in lock and split response [processor retry; col. 48, lines 7-24].

As per claim 7, Thaller discloses a plurality of masters [e.g. plural modules].

### ***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 8-10, 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thaller in view of Jarmaillo (USPN 5872937).

As per claims 8, 9, 17, 18 and 19, Thaller discloses an arbiter [arbiter logic 256; fig. 3B]; and plural masters (plural modules); except for the multiplexer and present idle or control signal to the bus. Jarmaillo teaches in a system of optimizing bus arbitration latency to provide a multiplexer to present a transfer signal to the bus or idle signal [abstract]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to employ the multiplexer of Jarmaillo in the system of Thaller in that Jarmaillo states that such methodology would reduce arbitration latency thus optimizing bus efficiency and the overall efficiency of the computer system by speeding up the flow of data [col. 1, lines 35-42].

As per claim 10, the combination of Thaller and Jarmaillo teaches the claimed invention including detecting plethora of conditions of no masters and removing bus mastership for example, Jarmaillo states that bus grant idle state insertion logic allows immediate deassertion of all bus grant output signals [abstract] thus remove all bus mastership from the bus. Note, that PCI bus system allows retry or split transactions.

8. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over the AMBA Specification in view of Jarmaillo (USPN 5872937).

As per claims 1, 8, 9, 11, 17-19 and 20, AMBA Spec. discloses a system and method comprising: a bus; at least one master [chapter 3 and 4]; and a first circuit [arbiter] configured to (i) grant a bus mastership [chapters 3 and 4], (ii) present a first transfer signal to said bus

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[chapters 3 and 4] and (iv) present an idle transfer signal [chapter 3]. AMBA Spec. does not explicitly disclose as to the removing of bus mastership from the bus. Jarmaillo teaches in a system of optimizing bus arbitration latency to provide a multiplexer to present an idle transfer grant signal to the bus to enable deassertion of all bus grant output signals thus would remove all masterships from the bus [abstract]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to employ the multiplexer of Jarmaillo in the system of AMBA Spec. in that Jarmaillo states that such methodology would reduce arbitration latency thus optimizing bus efficiency and the overall efficiency of the computer system by speeding up the flow of data [col. 1, lines 35-42].

As per claims 2 and 12, AMBA Spec. discloses wherein (i) the first circuit is configured to detect [chapter 3] when zero masters of said at least one master are able to use the bus; and Jarmaillo teaches removing mastership from all masters [Abstract].

As per claims 3-6 and 13-16, AMBA Spec. discloses wherein the masters are involved in lock and split response [chapter 3].

As per claim 7, AMBA Spec and Jarmaillo, both disclose a plurality of masters.

As per claim 10, the combination of AMBA Spec. and Jarmaillo teaches the claimed invention including detecting plethora of conditions of no masters (AMBA Spec., chapters 3 and 4) and removing bus mastership; for example, Jarmaillo states that bus grant idle state insertion

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logic allows immediate deassertion of all bus grant output signals [abstract] thus remove all bus mastership from the bus. Note, that PCI bus system allows retry or split transactions as well as explicitly stated in the AMBA Spec.

***Conclusion***

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Frame et al. (USPN 5349690), Wade et al. (USPN 5613075), and Nadir (USPN 4257095) teach different arbitration techniques involving a plurality of bus masters.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to XUAN M. THAI whose telephone number is 703-308-2064. The examiner can normally be reached on Monday to Friday from 8:30 A.M. to 5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



XUAN M. THAI  
Primary Examiner  
Art Unit 2111